THAT WHICH IS CLAIMED IS:

1. A generator comprising an oscillator producing a clock signal (CKHF) from an N-bit control number (NR), N being an integer greater than 1, wherein the oscillator (40) comprises:

- a first group of cells comprising cells (C(1) to C(NH)), each cell having at least one series-connected inverter, and first selection means to select a variable number of cells of the first group of cells as a function of NH0 most significant bits of the control number (NR), and

- a second group of cells comprising cells (D(1) to D(NL)), each cell comprising at least one series-mounted inverter and second selection means to select one of the cells of the second group of cells as a function of NL0 least significant bits of the control number (NR),

the cells of the first group and the cell of the second group selected being series-mounted to form a chain of inverters.

2. A generator according to claim 1, wherein each cell (C(1) to C(NL)) of the second group of cells is assigned a place value j ranging from 1 to NL, and wherein the second selection means comprise NL switches (INTD(1) to INTD(NL)) controlled by signals (SDL(1) to SDL(NL)) representing NL0 least significant bits of the control number (NR), each switch (INTD(j)) being series-mounted with a cell having a same place value j between an input point (E) and an output point (S).

3. A generator according to claim 1, wherein two different cells of the second group of cells, having respective place values j, k, $j \neq k$, have different propagation times (TD0(j)+TD1(j), TD0(k)+TD1(k)) for a 0 and a 1.

4. A generator according to claim 1, wherein, the difference between the propagation time (TD0(j)+TD1(j)) of a 0 and a 1 in a cell with a place value j of the second group of cells and that of a cell (TD0(j-1)+TD1(j-1) with a place value j-1 is smaller than the relative uncertainty (ΔP) sought for the period of the clock signal (CKHF) obtained.

5. A generator according to claim 1 wherein, when the control number (NR) increases by 1, a cell (D(j)) with a place value j of the second group is selected, this selected cell being:

- the cell with the place value immediately higher than that of a previously selected cell (D(j-1)), or

- the cell with a lower place value (D(1), an additional cell of the first group of cells (C(I+1) being in this case also selected.

6. A generator according to claim 1, also comprising a comparator (32) to compare the period (PHF) of the clock signal with a desired period and give the control number (NR) in the form of N logic signals (S(1), the control number varying as follows:

- the control number (NR) increases if the period (PHF) of the clock signal (CKHF) is smaller than the desired period (PHF0),

- the control number (NR) diminishes if the period (PHF) of the clock signal (CKHF) is greater than the desired period (PHF0),

- else the control number (NR) is constant.

7. A generator according to claim 1, also comprising a first decoder (34) to decode the NL0 least significant bits of the control number (NR) and give a first set of NL = 2^{NL0} control signals (SDL(1) to SDL(NL)) to the second selection means, this first set of control signals having the following properties:

- SDL(j) = 1 if j = NRL+1 for any value of j ranging from 1 to NL, NRL corresponding to the decimal value of the NL0 least significant bits of the control number (NR).

8. A generator according to claim 1, also comprising a second decoder (36) to decode the NH0 most significant bits of the control number (NR) and give the first selection means a second set of NH = 2^{NH0} control signals (SDH(1) to SDH(NH)) having the following properties:

- SDH(i) = 1 if i = NRH+1 for any value of i ranging from 1 to NH, NRH corresponding to the decimal value of the NH0 most significant bits of the control number (NR).

9. A generator according to claim 1, also comprising a control circuit (50) to verify the following inequality:

$$0 \leq (TC0+TC1) + (TD0(1)+TD1(1))-(TD0(NL)+TD1(NL))$$

TC0+TC1 being the propagation time of a 0 and a 1 in a cell of the first group of cells,

TD0(1)+TD1(1) being the propagation time of a 0 and a 1 in the least significant cell (D(1)) of the second group of cells,

TD0(NL)+TD1(NL) being the propagation time of a 0 and a 1 in the most significant cell (D(NL)) of the second group of cells,

the control circuit producing a first control signal (Cde(NL)) if the inequality is not verified.

10. A generator according to claim 9, wherein the control circuit (50) comprises:

- a reference oscillator (OSCref), to produce a clock signal with a reference period proportional to (TC0+TC1) + (TD0(1)+TD1(1)),

- a first measurement oscillator (OSC(NL)) to produce a clock signal having a measured period proportional to (TD0(NL)+TD0(NL)), and

- a first comparison circuit (COMP(NL)) to compare the measured period with a reference period and give the first active control signal (Cde(NL)) if the measured period is smaller than the reference period.

11. A generator according to claim 9, wherein the comparator (32) increases the control number (NR) by one unit when it receives the control signal (Cde(NL)).

12. A generator according to claim 10 wherein, to verify the inequality :

$0 \leq (TC0+TC1)+(TD0(1)+TD1(1))-(TD0(NL-1)+TD1(NL-1))$,

TC0+TC1 being the propagation time of a 0 and of a 1 in a cell of the first group of cells,

the control circuit also comprises:

- a second measurement oscillator (OSC(NL-1)) to produce a clock signal having a second measured period proportional to (TD0(NL-1)+TD1(NL-1)), and

- a second comparison circuit (COMP(NL-1)), to compare the second period with the reference period and give a second active control signal (Cde(NL-1)) if the measured period is smaller than the reference period.

13. A generator according to one of the claims 10 to 12, wherein the control circuit is activated when the oscillator starts, the first control signal (Cde(NL)) and/or the second control signal (Cde(NL-1)) produced by the control circuit being memorized.

14. A generator according to claim 13, wherein the first control signal (Cde(NL)) is taken into account only when the cell (D(NL-1)) with the place value NL-1 of the second group of cells is selected.

15. A generator according to claim 13, wherein the second control signal (Cde(NL-1)) is taken into account only when the cell (D(NL-2)) with the place value NL-2 of the second group of cells is selected.

16. A generator according to one of the claims 10 to 12, wherein the control circuit is activated whenever the cell (D(NL-1)) with the place value NL-1 of the second group of cells is selected.

17. A generator according to one of the claims 10 to 12, wherein the control circuit is activated whenever the cell (D(NL-2)) with the place value NL-2 of the second group of cells is selected.